UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	001344	Total Pages	
First Named Inventor or Application Identifier			
Shinsuke NAKAJYO, Yoshiyuki YONEDA and Hideharu SAKODA			
Express Mail Label No.			

Check Box, if applicable [ ] Duplicate

APPLICATION ELEMENTS FOR:
MANUFACTURE OF WAFER LEVEL SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

ADDRESS TO: Director of Patents and Trademarks
BOX PATENT APPLICATIONS
Washington, D.C. 20231

1. [XX] Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)

2. [XX] Specification Total Pages [17]

3. [XX] Drawing(s) (35 USC 113) Total Sheets [5]

4. [XX] Oath or Declaration Total Pages [5]

a. [XX] Newly executed (original)

b. [ ] Copy from prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [XX] Power of Attorney

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No. 001344
	First Named Inventor or Application Identifier
	Shinsuke NAKAJYO, Yoshiyuki YONEDA and Hideharu SAKODA
	PAGE 2 OF 3

10. [ ] English translation Document (if applicable)

11. [ ] Information Disclosure Statement [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [XX] Return Receipt Postcard (MPEP 503)

14. [ ] Small Entity Status is claimed.

15. [ ] Claim for Convention Priority [ ] Certified copy of Priority Document

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119.
The certified copies/copy have/has been filed in prior application Serial No. _____.
(For Continuing Applications, if applicable).

16. [ ] Other _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

[ ] Continuation [ ] Division [ ] Continuation-in-part (CIP) of prior application no. _____/_____

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic . . Fee $710.00
Total Claims	8 - 20		x $18.00	
Independent Claims	5 - 3	2	x $80.00	$ 160.00
Multiple Dependent Claims			$270.00	$ 270.00
			Basic Filing Fee	$1140.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			$40.00	$ 40.00
TOTAL				$1180.00

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	001344
	First Named Inventor or Application Identifier	
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	PAGE 3 OF 3	

[XX] A check in the amount of $ 1180.00 is enclosed to cover the filing fee of $ 1140.00 and the assignment recordation fee of $40.00.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of _____ to cover the filing fee and the _____ assignment recordation fee. A duplicate of this sheet is attached.

[XX] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

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Signature	Ronald F. Naughton	Date: October 12, 2000

RFN/ll

TITLE OF THE INVENTION

MANUFACTURE OF WAFER LEVEL SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

DETAILED DESCRIPTION OF THE INVENTION

Background of the Invention

The present invention relates to a method of manufacturing wafer level semiconductor device and a semiconductor device wherein a plurality of chips and chip size packages (hereinafter referred to as CSP) are formed on the wafer and substrate.

There has been proposed a semiconductor package having the structure that an external output terminal formed of a projected electrode is provided on a chip, in order to provide the shape of semiconductor package sealed with resin closely to a semiconductor element (hereinafter referred to as chip) as much as possible, at least the side surface of projected electrode is sealed with resin under the wafer condition and thereafter each chip is diced. (Japanese Published Unexamined Patent Application No. HEI 10-79362; US Patent application No. 09/029,608)

The present invention relates to a method for providing manufacturing history used to conduct failure search of such wafer level semiconductor device and a semiconductor device manufactured using such method.

Information including manufacturer name, type, manufacturing lot or the like has been marked on the resin of a semiconductor device surface in the semiconductor device of the type other than the wafer level semiconductor device, namely the semiconductor package after the dicing and resin sealing. If a failure has

occurred, history of manufacturing lot can be searched from this marking information and thereby cause of fault can be identified effectively.

The similar information is also marked in the wafer level semiconductor device of the related art.

In manufacture of semiconductor device using wafer including wafer level semiconductor device, manufacturing processes are all performed under the wafer condition but a fault is sometimes generated from the particular position on the wafer. In this case, it is required to detect where a fault is generated on the wafer but since no marking is conducted on the chip in the manufacturing method of the related art, it is impossible to identify where a fault has occurred on the wafer.

Even if marking is conducted on the chip, it is required to execute the process to melt the resin and it is considerably complicated to confirm the marking after the sealing with resin.

Brief Summary Of The Invention

Therefore, it is an object of the present invention to provide a method of manufacturing semiconductor device in the method of manufacturing wafer level semiconductor device where a fault can be searched from the marked information even after the sealing resin is formed on the wafer and a semiconductor device manufacturing with such semiconductor device manufacturing method.

The object of the invention is achieved by a method of manufacturing wafer level semiconductor device, comprising sealing process for sealing, with resin material, the front surface of a wafer having the front and rear surfaces and having formed a plurality

of semiconductor chips on the front surface, first marking process for marking the position information corresponding to each chip in the region of each chip at the rear surface of the wafer, process for conducting electrical test to each chip, second marking process for marking the result of the electrical test corresponding to each chip in the region of each chip at the rear surface of the wafer, and dicing process for dicing each chip.

Further, the object of the invention is achieved by a method of manufacturing wafer level semiconductor device comprising sealing process for sealing, with resin material, the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface thereof, process for conducting electrical test to each chip, marking process for marking, in the region of each chip at the rear surface of the wafer, the position information corresponding to each chip and the result of the electrical test, and dicing process for dicing each chip.

Further, the object of the invention is achieved by a method of manufacturing wafer level semiconductor device comprising sealing process for sealing, with resin material, the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface, attaching process for attaching, to the rear surface of wafer, a resin sheet on which marking is made on the wafer to indicate position of each chip and dicing process for dicing each chip.

Further, the object of the invention is achieved by a semiconductor device comprising a semiconductor chip diced from the predetermined position of wafer wherein circuits are formed

at the front surface, a resin sealing the front surface of the semiconductor chip, an external output terminal exposed from the resin and connected with the circuits, and a marking provided at the rear surface of the semiconductor chip to indicate the predetermined position of the wafer.

Further, the object of the invention is achieved by a semiconductor device comprising a semiconductor chip diced from the predetermined position of a wafer where circuits are formed at the front surface, a resin for sealing the front surface of the semiconductor chip, an external output terminal exposed from the resin and connected to the circuit, resin sheet attached to the rear surface of the semiconductor chip and a marking for indicating the predetermined position of the wafer printed on the resin sheet.

Each means described above includes following operations.

According to the first manufacturing method described above, resin sealing and electrical test are performed under the wafer condition without dicing individual chips from the wafer and therefore wafer manufacturing record can easily be corresponding to the chip manufacturing record. Moreover, marking can be made in the wafer condition before individual chips are diced into each chip. Therefore, when the manufacturing information is described at the time of marking, the chip manufacturing record is also left together with the position information on the wafer of chip to individual chip after the dicing in such a case that the manufacturing information is described at the time of marking. Thereby, if a defective product is generated, the cause may be searched easily and trace-ability can be improved.

According to the second manufacturing method described above,

since the marking of position information can be executed in the same process as the marking of the result of electrical test, effective marking may be realized by attempting twice the marking process as described in the first method.

According to the third manufacturing method described above, since the resin sheet is used, the semiconductor package on which at least position information is marked can be structured only by attaching the resin sheet and the making can be done within a short period of time.

According to the first semiconductor device as described above, the information suggesting where the chip in the semiconductor package is located during the manufacturing process is marked and the manufacturing location record is left and therefore if a fault is generated, the cause of such fault may be searched easily and thereby trace-ability can be improved.

According to the second semiconductor device as described above, since the resin sheet is used in addition to the operation effect similar to that of the first device, the semiconductor package on which the position information is marked can be obtained at a low price.

BRIEF DESCRIPTION OF THE DRAWING

The object and advantages of the invention will become apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawing of which:

Fig. 1 is a diagram for explaining the manufacturing process of the first embodiment of the present invention.

Fig. 2 is a diagram for explaining the manufacturing process of the first embodiment of the present invention.

Fig. 3 is a diagram for explaining the manufacturing process of the first and second embodiments of the present invention.

Fig. 4 is a diagram for explaining the manufacturing process of the third embodiment of the present invention.

Fig. 5 is a diagram for explaining the manufacturing process of the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, a preferred embodiment of the method of manufacturing wafer level semiconductor device of the present invention will be explained with reference to Fig. 1 to Fig. 5.

The wafer level semiconductor device used in the present invention provides an external output terminal formed of a projected electrode composed of Cu or the like to the electrode on each chip of wafer and is resin-sealed at its side surface of at least projected electrode under the wafer condition. Moreover, the wafer level semiconductor device of the present invention forms a plurality of chip at the surface thereof by the well known wafer process and those where a plurality of CSPs are formed on the substrate and these are resin-sealed at a time are also included in the wafer level semiconductor device.

(First Embodiment)

Figs. 1(a) and 1(b) are diagrams for explaining the first embodiment of the present invention indicating the resin sealing process of the wafer level semiconductor device of the first

embodiment.

In these figures, numeral 1 designates a semiconductor wafer where a plurality of CSPs or ordinary chips are formed. In more detail, this semiconductor wafer is disclosed in the Japanese Published Unexamined Patent Application No. HEI 10-79362.

On the chip or CSP formed on the wafer 1, pad electrodes are formed and the projected electrode (hereinafter called a post) is formed thereon as the external output terminal formed of copper or the like. On the circuit surface of wafer 1, the sealing resin is formed to protect the chip formed on the wafer surface.

The sealing resin is formed in the following processes.

As illustrated in Fig. 1(a), the wafer 1 is placed in the cavity formed of an upper metal die 5 and a lower metal die 6. This cavity is formed a little larger than the wafer in size. The sealing resin is formed on the wafer by compression molding of the resin between the upper metal die 5 and lower metal die 6. But, a temporary film 4 is provided in the upper metal die to easily separate the metal dies on the occasion of taking the wafer from the metal dies.

Fig. 1(b) illustrates the process to form a sealing resin 3 to the wafer set in the metal dies of (a) through the compression mold of resin.

In order to mold the sealing resin 3, a resin tablet (not illustrated) is placed first at the center of wafer, pressure is then applied to the upper and lower metal dies under application of heat, and the resin tablet is widened on the wafer 1 to conduct the compression mold. Thereby, the sealing resin 3 is formed covering the circuit surface and side surface of the wafer. In place of the compression mold explained above, the resin sealing

can be realized also using the ordinary transfer mold.

Next, the process to conduct marking, test and dicing to the wafer having completed the resin sealing will be explained with reference to Figs. 2(a) to 2(d) and Fig. 3(a).

Fig. 2(a) illustrates the wafer under the condition having completed the resin sealing explained above. The marking of position information is performed in the process (b) to the region of each chip at the rear surface of chip for the rear surface 3 of the wafer in the opposite side of the circuit surface of this wafer to form the marking 2a. These processes correspond to the steps 41, 42 illustrated in Fig. 3(a).

Position information indicates where the chip to be marked is located on the wafer. For example, when the virtual X-Y axis is provided to the wafer and the numerals corresponding to such coordinates are marked, the position information on the wafer can be indicated in each chip.

In addition to the marking of the position information, the basic information including type of product, lot number and manufacturing week can also be marked here.

Moreover, this information can be marked based on the assembling information stored in an assembling information storage memory 48 (Fig.3(a)) in regard to the fault generated at the time of resin sealing. This assembling information includes the position information indicating where the partial fault of sealing resin generated at the time of compression mold is located on the wafer.

The mark 2 may be printed using the laser. The YAG laser or green laser is used and output of this laser is set to 300 to

500 mW.

Next, as illustrated in Fig. 3(c), electrical test is performed in the wafer level for each chip. Chip test is conducted by placing the probe pin 12 in contact with the Cu post 10 as the external electrode formed on each chip. The probe pin 12 may be placed in contact in unit of several pins and placed simultaneously with all pins of the chip. Moreover, the probe pin 12 may be placed in contact with a plurality of chips or the wafer contactor may be used for simultaneous contact to all wafers. These processes correspond to the step 43 illustrated in Fig. 3(a).

Electrical test is performed to confirm whether the internal circuit functions in correct or not for each chip and the burn-in test may also be performed as required under the predetermined temperature environment.

Result of this electrical test is stored in the test information storage memory 49. In this case, data of good product is stored together with the position information to form the good product map data.

Thereafter, as illustrated (d), result of the electrical test is marked in the region of each chip at the rear surface of the wafer to form the mark 2b. This process corresponds to the step 44 illustrated in Fig. 3(a).

Result of this test may be performed to indicate good product or defective product or to indicate only the good product. Moreover, this marking may be performed for the good product in the predetermined ranks.

Finally, as illustrated in (d), dicing is conducted for each chip using a dicing saw and as illustrated in (e), individual

semiconductor package can be obtained. Only the good product of the semiconductor package are selected and delivered on the basis of the marked information explained above. These processes correspond to the steps 45, 46, 47 illustrated in Fig. 3(a).

For this selection, the good product map data explained above is used and selection of only good product can be traced for confirmation by referring to the map data based on the position information within the wafer. Moreover, the defective product may be discriminated easily by giving thereto the marking that enables visual discrimination from the good product.

As explained above, since the resin sealing and electrical test are performed under the wafer condition without dicing of each chip from the wafer, the wafer manufacturing record may be easily set to correspond to the chip manufacture record. Moreover, according to the present embodiment, marking can be done under the wafer condition before the each chip can be isolated with the dicing process. Therefore, when the manufacturing information is described at the time of marking process, the chip manufacturing record is also left together with the position information on the wafer of individual chip after the dicing process and thereby the cause may easily be traced if a fault is generated, thus improving the trace-ability in the failure search.

(Second Embodiment)

Fig. 3(b) is a diagram illustrating the second embodiment of the present invention.

Difference from Fig. 3(a) lies in that the marking of position information is not performed before the electrical test 52 in the wafer level but after this test.

As explained above, in this embodiment, since the marking of the position information and marking of the result of electrical test are conducted in the same process, this marking can be realized more effectively than the two times of markings as illustrated in Fig. 3(a).

(Third Embodiment)

Fig. 4 is a diagram illustrating the third embodiment of the present invention.

This embodiment suggests the sealing of both surfaces of the wafer with the resin 3a, 3b as illustrated in Fig. 2.

As illustrated in (a), the circuit surface side is sealed with the resin 3a, while the opposite surface with the resin 3b. This sealing process can be conducted by conducting twice the method explained in Fig. 1 through upside down of the wafer.

Next, as illustrated in (b), the marking of position information is performed to the resin 3b in the opposite side of the circuit surface as in the case of the first embodiment to form the mark 2.

Next, as illustrated in (c), the electrical test is performed, as in the case of the first embodiment, by placing the probe 12 in contact with the Cu post 10 exposed from the resin 3a at the circuit surface.

Finally, as illustrated in (d), the result of electrical test is marked to the resin 3b as in the case of t he first embodiment. The remaining processes may be performed in the same manner as the first embodiment.

The marking process may be performed, as in the case of the second embodiment, by simultaneously marking both position

information and result of electrical test.

As explained above, marking can be performed to the resin surface with the existing facilities for printing the mark on the resin surface by sealing the both surfaces of wafer with resin and then printing the mark on the resin surface.

(Fourth Embodiment)

Fig. 5 is a diagram for explaining the fourth embodiment of the present invention.

In this embodiment, the circuit surface and opposite surface of the wafer explained in Fig. 4 are formed of a resin sheet 7 of heat-resistant organic material, for example, polyimide.

First, the circuit surface side is sealed with the resin 3a.

Next, the position information is marked on the resin sheet 7 as in the case of the first embodiment.

Next, as in the case of the first embodiment, the electrical test is performed by placing the probe in contact with the Cu post exposed from the resin 3a of the circuit surface and the result is marked on the resin sheet 7. Thereafter, this resin sheet is attached to the opposite surface of the circuit surface of wafer. The remaining processes are performed in the same manner as the first embodiment for the dicing of wafer to each chip.

The semiconductor package having the marking can be formed only by attaching the resin sheet through the use of such resin sheet and the marking can be performed only within a short period of time.

In the marking process, it is also possible, as in the case of the second embodiment, to simultaneously mark both position information and result of electrical test on the resin sheet 7 and

thereafter attach the resin sheet having the marking to the rear surface of the wafer.

Thereby, the marking information including the position information and result of electrical test is not required to temporarily print unlike the first embodiment and the result of electrical test can be marked on the resin sheet simultaneously when the test is performed.

Moreover, it is also possible to previously print the numerals and codes indicating the position information of the chip on the resin sheet and then attaching the resin sheet to the rear surface of wafer under the condition of Fig.2(a). In this case, the result of electrical test is not printed. The result of electrical test is no longer required to print on the resin sheet in the case where such result is stored in the memory together with the position information of chip. Thereby, the marking process of the test result may be omitted and accordingly the processes may be saved.

[Effect of the Invention]

As explained above, according to the method of manufacturing wafer level semiconductor device of the present invention, sine the information indicating where the internal chips are located on the wafer can be printed on the diced semiconductor package, the trace-ability of search for defective product can be very much improved.

What is claimed is:

1. A method of manufacturing wafer level semiconductor device, comprising the steps of:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface with resin material;

a first marking the position information corresponding to each chip in the region of each chip at the rear surface of said wafer;

conducting electrical test to each chip;

a second marking the result of said electrical test corresponding to each chip in the region of each chip at the rear surface of said wafer; and

dicing the wafer into each chip.

2. A method of manufacturing wafer level semiconductor device comprising:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface thereof with resin material;

conducting electrical test to each chip;

marking in the region of each chip at the rear surface of said wafer, the position information corresponding to each chip and the result of said electrical test; and

dicing the wafer into each chip.

3. A method of manufacturing wafer level semiconductor as claimed in claim 1 or 2, wherein the circuit surface of said wafer and the opposite surface thereof are sealed with resin material and said position information and result of electrical test are marked in the region of each chip on the surface.

4. A method of manufacturing wafer level semiconductor device comprising:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on said front surface with resin material;

attaching a resin sheet on which marking is made on said wafer to said rear surface of wafer to indicate position of each chip; and

dicing the wafer into each chip.

5. A method of manufacturing wafer level semiconductor device as claimed in claim 4 further comprising:

conducting electrical test to each chip; and

marking the result of said electrical test corresponding to each chip to the region of each chip of the rear surface of said wafer.

6. A semiconductor device comprising:

a semiconductor chip diced from the predetermined position of wafer wherein circuits are formed at the front surface;

a resin sealing the front surface of said semiconductor chip;

an external output terminal exposed from said resin and connected with said circuits; and

a marking provided at the rear surface of said semiconductor chip to indicate the predetermined position of said wafer.

7. A semiconductor device comprising:

a semiconductor chip diced from the predetermined position of a wafer where circuits are formed at the front surface;

a resin sealing the front surface of said semiconductor chip;

an external output terminal exposed from said resin and connected to said circuit;

a resin sheet attached to the rear surface of said semiconductor chip; and

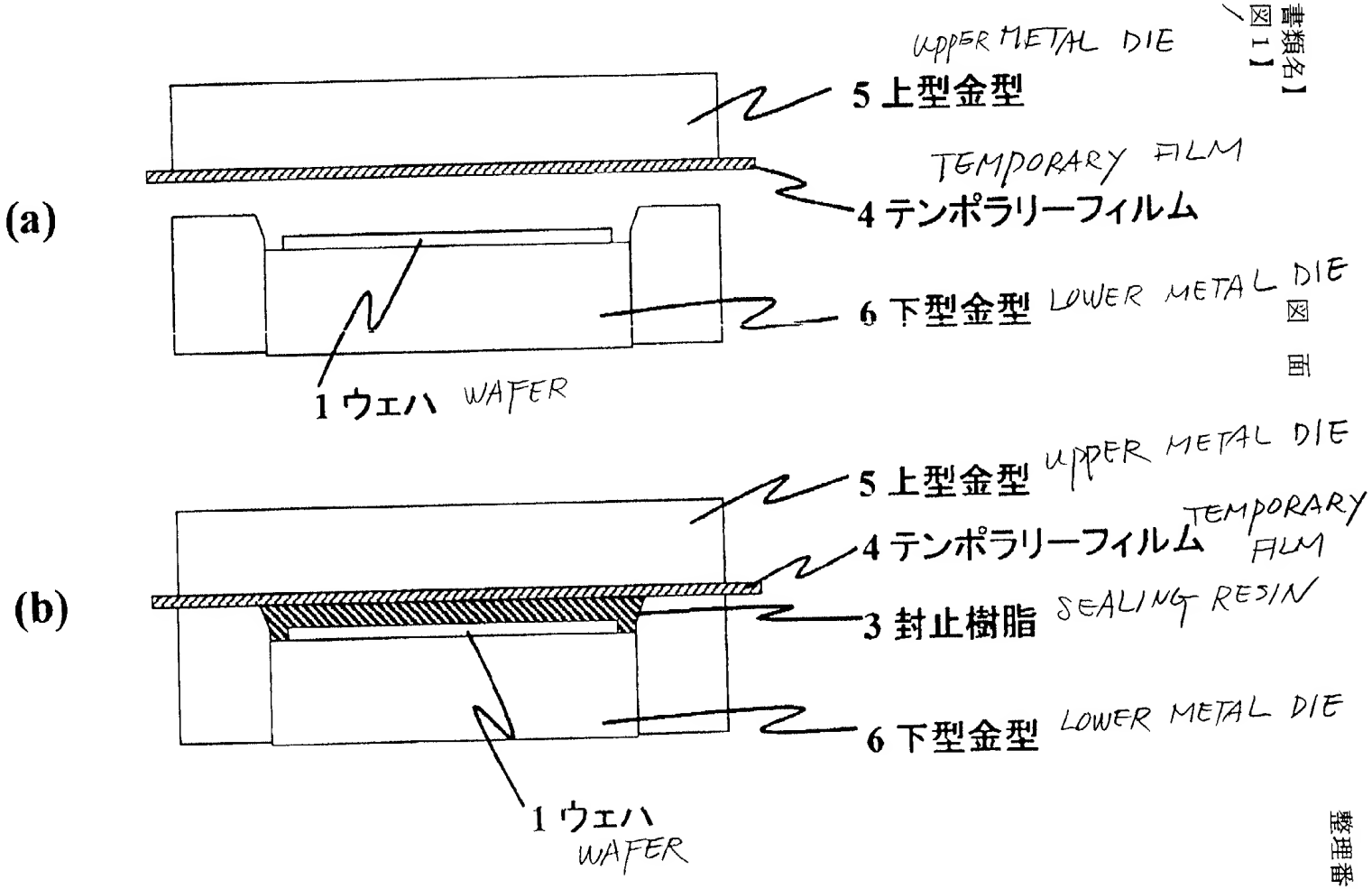
a marking indicating the predetermined position of said wafer printed on said resin sheet.

[ABSTRACT]

The object of the present invention is to provide a method of manufacturing semiconductor device in the method of manufacturing wafer level semiconductor device that can search the defective products from the marking information even when sealing resin is formed on the wafer and a semiconductor device manufactured with the same method. The means for solving the object is a method of manufacturing wafer level semiconductor comprising a process to seal with a resin material the surface of wafer having the front surface and rear surface and forming a plurality of semiconductor chips on said front surface, a first marking process for marking the position information corresponding to each chip to the region of each chip at the rear surface of said wafer, a process for performing the electrical test to each chip, a second marking process for marking the result of said electrical test to the region of each chip at the rear surface of said wafer and a dicing process for dicing the wafer to each chip.

【書類名】
【図1】

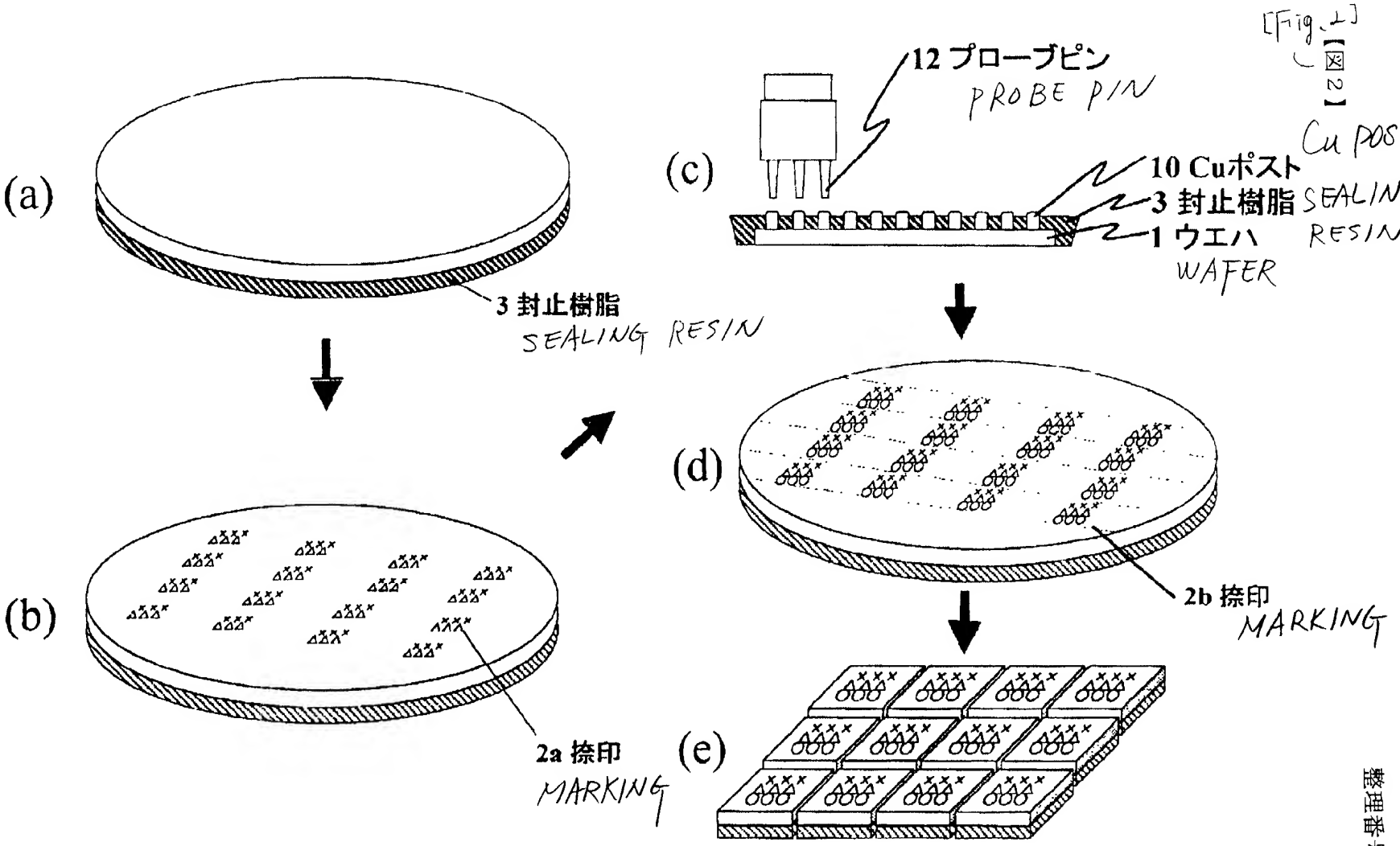
Fig. 1



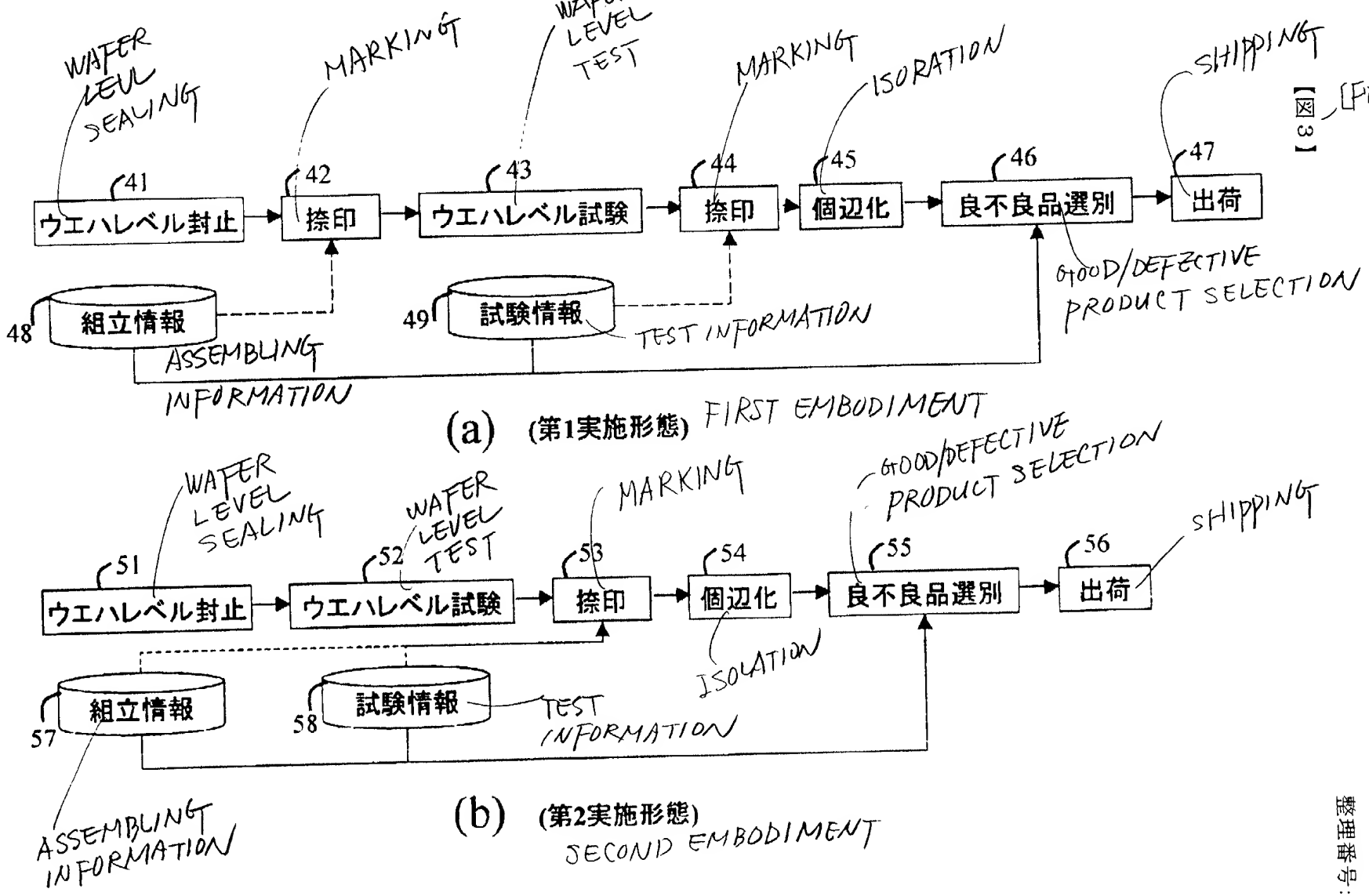
図面

整理番号:00-40650

[Fig. 1]【図２】


(a)
3 封止樹脂
SEALING RESIN
(b)
2a 捺印
MARKING
(c)
12 プローブピン
PROBE PIN
10 Cuポスト
Cu POST
3 封止樹脂
SEALING RESIN
1 ウエハ
WAFER
(d)
2b 捺印
MARKING
(e)

【図3】 [Fig.3]


WAFER LEVEL SEALING
MARKING
WAFER LEVEL TEST
MARKING
ISORATION
SHIPPING
41
42
43
44
45
46
47
ウエハレベル封止
捺印
ウエハレベル試験
捺印
個辺化
良不良品選別
出荷
GOOD/DEFECTIVE PRODUCT SELECTION
48
組立情報
ASSEMBLING INFORMATION
49
試験情報
TEST INFORMATION
(a) (第1実施形態) FIRST EMBODIMENT
WAFER LEVEL SEALING
WAFER LEVEL TEST
MARKING
GOOD/DEFECTIVE PRODUCT SELECTION
SHIPPING
51
52
53
54
55
56
ウエハレベル封止
ウエハレベル試験
捺印
個辺化
良不良品選別
出荷
ISOLATION
57
組立情報
58
試験情報
TEST INFORMATION
ASSEMBLING INFORMATION
(b) (第2実施形態)
SECOND EMBODIMENT

【図4】

[Fig. 4]

(a)
3b
3a
SEALING
封止樹脂
(b)
2 捺印
MARKING
(c)
12 プローブピン
PROBE PIN
10 Cuポスト Cu POST
3a
1 ウエハ WAFER
3b
(d)
RESIN
(e)

【図5】

[Fig. 5]

7 樹脂シート
RESIN SHEET
INFORMATION
MARKING
MANUFACTURING
捺印、製造情報
ISOLATION
個辺化
3a 封止樹脂
SEALING RESIN
1 ウエハ
WAFER

Declaration and Power of Attorney for U.S. Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

☐ 下記の名称の発明に関して請求範囲に記載され、特許出願されている発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者である（下記の名称が複数の場合）と信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MANUFACTURE OF WAFER LEVEL SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

2000-201416	Japan	3/7/00	Priority Not Claimed 優先権主張なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*
See list of attorneys and/or agents on page 5.

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（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

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第六共同発明者		Full name of sixth joint inventor, if any
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